Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-218 (canceled)

219. (currently amended) A chip package comprising:

a preformed substrate comprising semiconductor material~~, said preformed substrate having no circuitry~~;

only one preformed die joined with said preformed substrate; [[and]]

a first insulating layer comprising a first portion over said only one preformed die and a second portion over said preformed substrate but not over said only one preformed die, wherein said first insulating layer comprises polyimide; and

a first patterned circuit layer [[line]] over said first insulating layer, ~~only one preformed die and over said preformed substrate.~~

220. (currently amended) The chip package in claim 219, wherein said preformed die ~~comprising~~ comprises a first trace ~~thin-film circuit layer~~ formed therein, and wherein said first patterned circuit layer comprises a second trace [[line]] having a thickness greater than that of said first trace, ~~thin-film circuit layer.~~

221. (currently amended) The chip package in claim 219, wherein said first patterned circuit layer [[line]] comprises a power bus.

222. (currently amended) The chip package in claim 219, wherein said first patterned circuit layer [[line]] comprises a ground bus.

223. (currently amended) The chip package in claim 219, wherein said first patterned circuit layer [[line]] connects multiple portions of said only one preformed die.

Claims 224-227 (canceled)

228. (currently amended) The chip package in claim 219 further comprising ~~an~~ a second insulating layer over said first patterned circuit layer [[line]].

229. (currently amended) The chip package in claim 228, wherein said second insulating layer comprises polyimide.

230. (currently amended) The chip package in claim 228, wherein said second insulating layer comprises benzocyclobutene (BCB).

231. (currently amended) The chip package in claim 228, wherein said second insulating layer comprises a porous chip package.

232. (currently amended) The chip package in claim 219 further comprising ~~an~~ a second insulating layer on said first patterned circuit layer [[line]] and ~~further comprising another~~ a second patterned ~~line~~ circuit layer on said second insulating layer.

233. (currently amended) The chip package in claim 232, wherein said second insulating layer comprises polyimide.

234. (currently amended) The chip package in claim 232, wherein said second insulating layer comprises benzocyclobutene (BCB).

235. (currently amended) The chip package in claim 232, wherein said second

insulating layer comprises a porous chip package.

236. (currently amended) The chip package in claim 219 further comprising a capacitor ~~passive device~~ over said preformed substrate.

Claim 237. (canceled)

238. (currently amended) The chip package of claim 219 ~~236~~ further comprising an inductor over said first insulating layer.~~, wherein said passive device comprises an inductor.~~

239. (currently amended) The chip package of claim 219 ~~236~~ further comprising a resistor over said first insulating layer.~~ wherein said passive device comprises a resistor.~~

240. (currently amended) The chip package of claim 219 ~~236~~ further comprising a filter over said first insulating layer.~~, wherein said passive device comprises a filter.~~

241. (currently amended) The chip package of claim 219 ~~236~~ further comprising a wave guide over said first insulating layer.~~, wherein said passive device comprises a wave guide.~~

242. (currently amended) The chip package of claim 219 ~~236~~ further comprising a micro electronic mechanic element over said first insulating layer.~~, wherein said passive device comprises a micro electronic mechanical sensor (MEMS).~~

Claims 243-249. (canceled)

250. (currently amended) The chip package of claim 219, ~~243,~~ wherein an opening

[[is]] in said preformed substrate [[and]] accommodates said only one preformed die.

251. (previously presented) The chip package of claim 250, wherein said only one preformed die has a top surface substantially coplanar with that of said preformed substrate.

252. (currently amended) The chip package of claim 219, wherein said preformed substrate comprises a first layer and a second layer, said first layer being on said second layer, an opening ~~being~~ in said first layer ~~and~~ exposing said second layer[[,]] and accommodating said only one preformed die~~, being in said opening.~~

253. (previously presented) The chip package of claim 252, wherein said first layer comprises semiconductor material.

254. (previously presented) The chip package of claim 252, wherein said first layer comprises silicon.

255. (previously presented) The chip package of claim 252, wherein said second layer comprises metal.

256. (previously presented) The chip package of claim 252, wherein said only one preformed die has a top surface substantially coplanar with that of said first layer.

257. (currently amended) The chip package of claim 219 further comprising a polymer ~~an insulating~~ layer over said preformed substrate and around said only one preformed die.

Claim 258. (canceled)

259. (currently amended) The chip package of claim 257, wherein said polymer ~~insulating~~ layer comprises epoxy.

260. (currently amended) The chip package of claim 219 further comprising a solder bump on said first patterned circuit layer[[line]].

Claim 261. (canceled)

262. (currently amended) The chip package of claim 260 further comprising a gold bump on said first patterned circuit layer.~~, wherein said bump comprises gold.~~

263. (currently amended) The chip package in claim 219, wherein said only one preformed die comprises multiple active devices, and said first patterned [[line]] circuit layer connects said multiple active devices.

264. (previously presented) The chip package in claim 219, wherein said preformed substrate comprises silicon.

265. (currently amended) The chip package in claim 219, wherein said first patterned circuit layer [[line]] comprises copper.

266. (currently amended) The chip package in claim 219, wherein said first patterned circuit layer is connected to said only one preformed die through an opening in said first insulating layer. ~~only one preformed die has an active surface and a backside surface, said preformed substrate being under said backside surface of said only one preformed die, and said patterned line being over said active surface of said only one preformed die.~~

267. (currently amended) The chip package in claim 219, wherein said first patterned circuit layer ~~line further~~ comprises a first portion over said only one preformed die and a second portion over said preformed substrate but not over said only one preformed die. ~~a portion not over said only one preformed die.~~